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APPLICATION FOR PATENT

LCD DRIVING SYSTEM WITH LOW POWER REQUIREMENTS

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CROSS REFERENCE TO RELATED APPLICATION

This application is a continuation-in-part of U.S. Patent Application Serial No. 09/561,737, filed April 28, 2000, which is incorporated by reference in its entirety.

BACKGROUND OF THE INVENTION

This invention relates in general to liquid crystal displays (LCDs) and, in particular, to a low power driving scheme for LCDs.

Fig. 1 is a schematic view of a LCD panel and its n row electrodes labeled COM 1, ...COM n in Fig. 1, and k column electrodes shown as vertical rectangles labeled SEG 1~SEGk in Fig. 1. Not shown in Fig. 1 (to simplify the figure) is a layer of liquid crystal material between the row and column electrodes. Each row electrode will overlap a column electrode when viewed in a viewing direction, where the overlapping portion of the two overlapping electrodes will define a pixel of the LCD panel. When an appropriate voltage is applied across a particular row and a particular column electrode, a portion of the liquid crystal layer at the pixel between the overlapping row and column electrodes controls the light transmission or reflective properties of such portion.

Fig. 2a is a graphical illustration of the Improved Alto-Pleshko (IAPT) waveform for the row (or COM) electrodes and column (or SEG) electrodes. Fig. 2b is a graphical plot of the conventional Alto-Pleshko driving waveform for row (COM) and column (SEG) electrodes. In Figs. 2a and 2b, voltages labeled V_{COM} or variations thereof indicate voltage waveforms that are applied to the row electrodes and voltages labeled V_{SEG} or variations thereof indicate voltage waveforms applied to column electrodes. The driving waveforms in Figs. 2a and 2b are conventional. Referring to Fig. 1 and Fig. 2a, a typical configuration of passive LCD and a conventional driving waveform is illustrated. As demonstrated in Fig. 1, the ith row electrode is connected to a node at voltage V_{COMi}, on one side, and the jth column electrode is connected to a node at voltage V_{SEGj} on the other side. In Fig. 2a, where vertical axis is voltage, and the horizontal axis time, the data signals V_{SEGj} are also drawn as

overlapped shaded region over V_{COMi} signal to illustrate relative relationships between these two sets of signals.

The driving waveform demonstrated in Fig. 2a, is known as Improved Alto-Pleshko driving method (Improved APT, or IAPT for brief). The main characteristic is that the COM scanning pulses are "folded" such that the driving total voltage dynamic range is reduced as compared to the plain APT, as show in Fig. 2b. This reduced voltage range is considered to be advantageous in the conventional design technique used in CMOS integrated driver IC, where low MOS transistor break down voltage (caused by thin gate oxide used in fine gate geometry circuits and devices) would otherwise make the circuit design very difficult.

From the waveform of these signals it is observed that although the IAPT driving method reduces the voltage dynamic range for the drivers, but the power is increased as a consequence. This is because the LCD is a pure AC device and the capacitive load on column (SEG) electrodes can be quite significant. However, the current driving the column (SEG) electrodes also need to flow through the entire voltage range, although the column (SEG) electrode voltage swing, *V6 - V4*, or *V3 - V1* as shown in Fig. 2a (these two value needs to be the same), as measured from "majority" COM electrode voltage (which is substantially the same as the non-scanning voltage V_5 in Field 2xN and V_2 in Field 2xN+1) is far smaller than the total supply voltage used in a conventional IAPT driving scheme (*V6 - V1* in Fig. 2a.).

According to conventional design principal, the ratio between (*V6 - V1*) and (*V3 - V1*) can be estimated roughly by $\sqrt{\frac{Mux+1}{2}}$, where Mux is the multiplexing rate (or duty factor), which is determined by the number of row/COM electrodes. Using this formula, for a moderate sized LCD of 81 rows (with 81 row/COM electrodes), the above ratio is 5x, and therefore, the power wasted for driving SEG electrodes (which is proportional to voltage *V*, assuming current *I* stays unchanged) can be as high as 80%.

As there will be only one COM electrode scanning while all SEG electrodes can change at each row scanning period, SEG/column electrode capacitive loading current can be more than ten times higher than COM/row electrode loading current. This obviously makes the low utilization of supplied SEG/column power very undesirable.

One of the most frequently heard complaints from users of portable computers, cellular phones and personal digital assistants is that these devices consume too much power so that one has to constantly change batteries, which is inconvenient. It is, therefore,

desirable to provide a power saving scheme for driving LCD displays, especially for displays used in such portable devices.

Another problem encountered in conventional LCD is crosstalk caused by its driving circuit design. Many passive LCD devices are driven by means of Class B bias circuits. In such circuits, to minimize power consumption, both N and P transistors are in the OFF state when the output of the circuit is not used to drive electrodes. Therefore, when the Class B bias circuit is used to drive the column electrodes to target voltage values, as the electrical potential of the driven electrode approaches the target value, the output error is small so that the output stage of conventional operational amplifier driver circuits moves towards Class B bias, where both N and P type transistors are in the OFF state and there is therefore very weak driving power. This causes the driver circuit to be in high impedance state due to the high RC value of the load driven by the drive circuit. Therefore, the residual error (the difference between the voltage across the row and column electrodes at the pixel addressed and the target value) tends to persist for a long time through a number of row-scanning cycles, thereby causing crosstalk. In this context, a row scanning cycle is the time period taken for applying electrical potentials to cause pixels overlapping a row electrode to have the opportunity to change state.

It is therefore desirable to provide an improved LCD driving scheme where the above-described crosstalk problem is reduced or minimized.

SUMMARY OF THE INVENTION

This invention is based on the recognition that by using two separate power supplies to generate suitable electrical potentials for driving the row and column electrodes, the current driving the column (SEG) electrodes does not need to flow through the total supply voltage (*V6 - V1* in Fig. 2A), so that the power consumed by the LCD can be significantly reduced. Preferably, one of the electrical potentials caused to be generated using the two power sources and applied to the row and column electrodes floats with the voltage supplied by one of the power sources. This allows the dynamic range of electrical potentials driving the LCD to be reduced, thereby also allowing the size of semiconductor devices in a power circuit to be reduced. This enables cheaper driver systems to be manufactured for driving LCD displays.

Since the LCD is a pure AC device, signal pulses driving the LCD will be higher than a reference voltage such as ground in some field addressing cycles (e.g. positive going pulses) and lower than the reference voltage (e.g. negative going pulses) in other field

addressing cycles. In one embodiment, by providing a voltage differential which is in turn used for generating both types of pulses, this ensures that no significant DC offset would develop across LCD pixels that can cause ionization of the liquid crystal material and damage the LCD permanently. In some embodiments, such voltage differential may be supplied directly by a voltage supply.

Preferably, an energy storage device is used in the low power driving scheme of this invention for generating electrical potentials suitable for driving the row and column electrodes. In a first phase of the operation of the scheme, one or more energy storage devices are charged, and in a second later phase, the energy stored is then used to drive the row and/or column electrodes. In some embodiments, power from the power sources may be used to both charge the energy storage devices as well as to drive row and/or column electrodes during the first phase.

In embodiments where one or more energy storage devices are employed, some of the current employed for driving the column electrodes in a field addressing cycle may be reused in a subsequent cycle for driving column electrodes.

Another aspect of the invention is based on the observation that, by using energy storage devices such as capacitors to drive the column electrodes, the above-described problems encountered with Class B bias circuits can be avoided altogether. Thus, if the energy storage device chosen has a much higher capacitance than the load it is driving, such as the capacitive load of the LCD pixels, it is possible to drive the column electrodes to a voltage close to or substantially at a target value within a row-scanning cycle, so that the above-described crosstalk problem associated with conventional drivers can be alleviated. In the preferred embodiment, two different energy storage devices may be used, with the first device used to drive the column electrode to a voltage close to but not at the target value, and the second device used to drive the column electrode then to substantially the target value, all within the same row-scanning cycle.

BRIEF DESCRIPTION OF THE DRAWINGS

Fig. 1 is a schematic view of a LCD panel and its row electrodes labeled COM 1, ...COM n in Fig. 1, and column electrodes shown as vertical rectangles labeled SEG 1~SEGk in Fig. 1.

Fig. 2a is a graphical illustration of the conventional Improved AltoPleshko (IAPT) waveform for the row or COM electrodes and column or SEG electrodes.

Fig. 2b is a graphical plot of the conventional Alto-Pleshko driving waveform for row (COM) and column (SEG) electrodes.

Fig. 3a is a schematic circuit diagram of a power supply circuit generating suitable electrical potentials for driving the row and column electrodes of a LCD to illustrate one embodiment of the invention.

Figs. 3b-3d are schematic circuit diagrams of portions of a power supply circuit generating electrical potentials suitable for driving the row and column electrodes of an LCD display to illustrate further embodiments.

Fig. 4a is a schematic circuit diagram of a power supply circuit for generating electrical potentials for driving a LCD with electrical potentials that float with a voltage supplied by a power supply to illustrate yet another embodiment of the invention.

Figs. 4b and 4c are graphical plots of signal waveforms employed in the embodiment of Fig. 4a.

Figs. 5a and 5b together illustrate a power supply circuit for generating electrical potentials suitable for driving the row and column electrodes of an LCD to illustrate a preferred embodiment of the invention.

Fig. 6a is a schematic circuit diagram of a power supply circuit for generating electrical potentials suitable for driving the column electrodes of a LCD to illustrate yet another aspect of the invention directed to the reduction of crosstalk.

Fig. 6b is a timing diagram of switching circuit waveforms and voltage waveforms to illustrate two different embodiments of the operation of the circuit in Fig. 6a.

For simplicity in description, identical components are labeled by the same numerals in this application.

DETAILED DESCRIPTION OF THE EMBODIMENTS

Referring to Fig. 2a and 2b, it is observed that in both IAPT (Fig. 2a) and APT (Fig. 2b) driving schemes, during the period of one field, such as field 2xN or field 2xN+1 in Figs. 2a, 2b (N being a positive integer), the SEG/column electrode voltage swings have a very limited dynamic range as compared to the COM/row electrode voltage swings. This invention involves the use of separate power supply systems to provide narrow range, voltage power supply for SEG/column drivers, and wide range voltage power supply for the COM/row drivers.

Floating V_{COM} Embodiments

In an embodiment of the invention for obtaining the signals illustrated in Fig. 2b, one floating high voltage V_{COM} supply or two fixed high voltage V_{COM} supplies can be used for the COM electrodes (discussed below). Either way, due to the fact that the current used to supply power the column electrodes are driven through a very limited dynamic range, this causes the power consumption of such a modified system to be lower than the conventional one-power supply driving systems by as much as 80% (see calculation above).

Floating V_{BIAS} Embodiments

In one embodiment of the invention for obtaining the signals illustrated in Fig. 2a, one floating low voltage supply system 12 in Fig. 3a provides electrical potentials $V_{B+}/V_0/V_{B-}$ that are used to supply the power for SEG/column switching. This V_{BIAS} supply 12, by proper control of switches, will be switching between three states:

Charge: where a power source, such as a charge pump or an buffer amplifier, is used to charge up capacitors connected between $V_{B+}/V_0/V_{B-}$ periodically. The capacitors then provide two "operating voltages" for driving the column electrodes.

V-Low: where the V_{B-} is connected to V1 and V_0/V_{B+} will provide V2, and V3.

V-High: where the V_{B+} is connected V6 and V_0/V_{B-} will provide V5, and V4.

As will be discussed in detail in the following paragraphs, a floating V_{COM} structure may be simpler than a floating V_{BIAS} structure. In addition, there will be some minor power consumption for switching V_{BIAS} between the three different states. However, a practical implementation of floating V_{COM} structure in a single chip CMOS IC implementation may call for the use of triple well CMOS process, while the floating V_{BIAS} structure can be achieved in the more conventional twin well CMOS process. Therefore the former approach (i.e. floating V_{COM}) is more suitable for larger LCDs where a multiple-chip solution is required to handle the driving loads, while the latter approach (i.e. floating V_{BIAS})is more suitable for smaller LCD where single chip solution is more economical.

Either of these two schemes will achieve very significant power savings compared to conventional single power supply system by utilizing the power more efficiently.

Floating V_{COM} Embodiments

Using Two Fixed V_{COM} supplies:

One of the embodiments of the invention involves the use of non-folding, APT driving scheme, (Fig. 2b) and utilizes two fixed V_{COM} supplies as illustrated in Fig. 3a and Fig. 3b. As will be understood by those in the art, while the driver circuit for driving only one row or column electrode is shown in the description below in reference to Figs. 3a-3d, 4a-4c and 5a, 5b, similar circuits may be employed for driving other row and column electrodes. While all of the column electrodes need to be driven at the same time, in some embodiments, only one row electrode is scanned at any one time, so that by means of a switching circuit, only one driver may be adequate for driving sequentially all of the row electrodes.

In Fig. 3a, the COM or row electrode is scanned by application of either $V0<=>V_{COM+}$ pulses or $V0<=>V_{COM-}$ pulses, depending on the polarity of the row being scanned. These pulses are supplied to the connection node COM of each row electrode by applying appropriate timing signals S+, S0, S- to control the switches I0, I1, I2. The driving potential V_{B+} or V_{B-} is applied to a connection node SEG for each column electrode by applying suitable timing signals SS+(j), SS-(j) to switches I3, I4. The notations "SS+(j), SS-(j)" indicate timing signals suitable for the jth column electrode, where j ranges from 1 to the maximum number of column electrodes. The power consumption of the system is very efficient as compared to conventional single power supply IAPT driving system. As the power consumed by the SEG/column electrodes will be supplied by a dedicated V_{BIAS} low voltage power supply, therefore the current loading of the SEG/column electrodes will have a lower V multiplier factor and therefore the system power requirements are reduced.

However, in this embodiment, V_{COM+}, V_{COM-} are permanently connected to the rest of the driver circuit and therefore require the switch circuit I0 and 12 to tolerate a breakdown voltage of $|V_{COM+} - V_{COM-}|$. Since $|V_{COM+} - V0| = |V0 - V_{COM-}| = V_{COM}$ and can be as high as 15~18V, the total breakdown requirement can be as much as 30~36V, which is quite expensive to achieve in fine geometry CMOS process. An improvement in this respect is therefore desirable.

Fig. 3b is a schematic view of a circuit diagram illustrating a portion of a power supply for generating electrical potentials suitable for driving a LCD. The portion of the power supply shown in Fig. 3b is for generating a suitable voltage for driving the row electrodes; the portion of the circuit used for generating electrical potentials for driving the column electrodes is similar to that of circuit block 12 of Fig. 3a. To simplify Fig. 3b, such

circuit block is omitted, it being understood that such circuit block is connected to node V0 of Fig. 3b in the same manner as shown in Fig. 3a. The same is true for Fig. 3c. In Fig. 3b, an improved scheme is illustrated. In this scheme, there are still two fixed high voltage supplies, V_{COM+} and V_{COM-}. However, two pairs of switches (I1/I5 and I4/I3) are used to select the power supply for all the row/COM electrode driving circuits. With these switches and the control signal F1a, F2a (where F1a is basically the inverse of F2a), according to APT driving technique, at any single time, only V_{COM+}, or only V_{COM-} is applied, but never both. As a consequence, the voltage across switches I0 and I2 will be limited to $|V_{COM}|$ rather than $2x|V_{COM}|$. For example in field 2N, only V0 and $V_{COM-}$are applied. The break down requirement is therefore reduced by two as compared to Fig. 3a embodiment. In addition, all four power supply switches (I5, I6, I7, I8) only went through one $|V_{COM}|$ transition, and therefore is also required to tolerate one V_{COM} for break-down tolerance.

The embodiment of Fig. 3b still requires two separate power supplies V_{COM+} and V_{COM-}. A further enhancement to Fig. 3b is show in Fig. 3c. In this embodiment, only one voltage supply V_{COM+} is used. In the positive cycle, signal F1a is High and switches I9, I11 are ON. The V+ connection node will connect to V_{COM+} and V- will connect to V0, while capacitor C0 will be charged to V_{COM+}. In the negative cycle, F2a will be high, switch I10 will be ON, and the electrical potentials from COM/row scanning system 20 is supplied by capacitor C0, which was charged to V_{COM+} during the positive cycle. With I10 turned ON, C0's top terminal is connected to V0, and therefore push C0's bottom terminal to $-V_{COM+}$, or V_{COM-}. As a result, by connecting different terminals of C0 to power supply V_{COM+} and to reference node V0, and using the other terminal as V_{COM+} or V_{COM-}, only one voltage source is required for the scanning of all row/COM electrode. This is possible because at any single moment in time, there will be only one row/COM electrode scanned in the APT driving scheme. This one single voltage source can supply the voltage required for both the polarity of row/COM scanning pulses.

This technique can be applied equally well to field inversion APT driving scheme (where the polarity will stay the same for all rows/COMs within one field, and change to another polarity for all rows/COMs for the next field), for row inversion APT driving schemes (where the polarity for one field will be + - + - + - for one field, and - + - + - + for the next field, etc.) or other inversion driving schemes. Another important advantage of this single V_{COM} scheme is the natural ability to provide balanced voltage supply to both of the polarity of driving signals. This balance is important as any significant DC offset applied across LCD pixels can cause ionization of the LC (liquid crystal) material and damage the

LCD permanently. By using only one supply voltage for V_{COM}, this balance is automatically established; otherwise, this may require additional high breakdown voltage feedback control circuits and may be difficult and costly to accomplish.

Yet another improvement to Fig. 3c is illustrated in Fig. 3d. In this embodiment, the connection to V0 is replaced by connection to V_{B+} and V_{B-}. In addition V_{B-} is connected to GND while V_{B+} is connected to one single power supply V_{B2}. This improved scheme further reduces the complexity of power supply for V_{B+}, V_{B-}. In addition, the connection of V_{COM} power supply to V_{B+} and V_{B-} allows the current used in supplying V_{COM} to flow through the storage capacitor for V_{B+} (and V_{B-}) and the capacitor formed by the row and column electrodes COMi, SEGj (shown in dotted lines in Fig. 3d) that are addressed at a particular pixel and be reused by the column/SEG electrode drivers for subsequent addressing. A further advantage of moving the V_{COM} connection away from V0 is that V0 serves the important role of establishing balance between V_{B+} and V_{B-} in order to minimize DC voltage as seen across pixel electrodes. If the loading of V_{COM} is through node V0, then all the row/COM scanning current will be loaded on V0, which make balancing more difficult to achieve and a strong voltage follower may be desirable to drive V0. When the V_{COM} is connected to V_{B+} and V_{B-}, V0 loading will come completely from column/SEG via LCD pixel capacitance coupling (e.g. COMi, SEGj in Fig. 3d), which is, by definition of capacitor coupling, DC free, and a device driving node V0 can be very weak (just enough to handle C_{B0} leakage and the unbalanced part of the coupled signals).

Current Reuse.

It will be noted that in Fig. 3b, 3c or 3d, the low voltage supply system V_{BIAS} involves the use of capacitor C_{B+} and C_{B-}. When a SEG electrodes swing from V_{B+} to V_{B-}, or vise versa, a current is coupled to the node V0 via the LCD panel capacitance. This current will be a "source" current (flowing out from V0 node) for V_{B+} to V_{B-} transition and "sink" current (flowing into V0 node) for V_{B-} to V_{B+} transition. As just discussed above, these currents are intrinsically balanced, and therefore result in no DC in the long term. Now, if a sufficiently large capacitor (for example over 150x the total LCD panel load capacitance) is connected between V0 and ground, then another very important characteristics will emerge, which is *current reuse*: the current used by one row of pixels for transitions from, say, V_{B+} to V_{B-} in one field will supply the same row's transition from V_{B-} to V_{B+} in the next field. Essentially, the current pulses will be used twice in two consecutive fields, but temporarily stored in the capacitor connected to V0. This is especially true for almost all passive LCD display

applications where the displayed image is essentially static and field to field image change is very limited. Another way of looking at the current reuse is to see the voltage being halved at each of the above transition (flowing first from V_{B+} to V0 and then from V0 to V_{B-} and the V0 will stay essentially unchanged, assuming the load current produce negligible DC drift on V0). In either perspective, the power consumption is cut in half by the C_{B+}/C_{B-} capacitor connected to V0.

Yet another aspect of this invention is related to the two capacitors C_{B+}/C_{B-} connected between V_{B+} to V0 and V0 to V_{B-}. The importance of C_{B-} in terms of current reuse has been discussed above. The significance of C_{B+} can be explained as follows. In order for the above current reuse scheme to work, the V0 node can not be "driven" within two consecutive filed (in other word, V0 can only be driven fairly infrequently, with an average frequency much lower than the field rate, ideally under 15~20 Hz, or about 20% of the field rate) and certain small percentage of V0 drifting (1~2%, +/- balanced) has to be allowed. This low frequency driving requirement is intrinsically conflicting with the requirement of V0 being the mid-point between V_{B+} and V_{B-}, which comes from the requirement of no net DC voltage being applied across pixel electrodes, as this will require V0 being controlled at all time.

The addition of C_{B+}, which is of substantially the same capacitance as C_{B-}, will therefore be important for the accomplishment of the current reuse scheme, as a capacitor voltage divider will be formed by C_{B-} and C_{B+}, and any fluctuation occurring across V_{B+} to V_{B-}, will automatically be reflected to V0 via the capacitor voltage divider, and therefore help V0 maintain its potential at $(V_{B+} - V_{B-})/2$. Without C_{B+}, the fluctuation of V_{B+} will be applied to only one side of V0 and a net DC voltage can easily develop across LCD pixels. Other than using an extremely precise voltage source for V_{B+}, which will be costly, the other way to overcome this DC problem is to use a fairly strong driver to fixate V0 at $(V_{B+} - V_{B-})/2$. Since this driver can not differentiate between unwanted drifting and the "good drifting" caused by currents to be reused, it may diminish any power savings, and render the current reuse scheme inoperable.

Floating VBIAS Embodiments

The above embodiments will achieve the desirable power saving by utilizing a separate power supply for SEG/column electrodes with the low voltage V_{BIAS}. However, due to the dual polarity nature of the circuit structure, the CMOS implementation of these schemes in a single chip LCD controller IC still requires the use of triple-well CMOS process (N-Well for P-MOS, when P-MOS operates in positive voltage, and P-Well for N-MOS,

when N-MOS operates in the negative voltage). Triple-Well CMOS process can be ~20% more expensive as compared to a otherwise equal twin-Well CMOS process (equal in terms of break down voltage, minimum geometry, layers of conductors, etc.). It is therefore desirable to modify the scheme to allow the more economical process to be used.

Referring the field-inversion IAPT driving scheme in Fig. 2a, it is observed that, during each field, the voltage swing of SEG/column is limited to a relatively smallvalue, on both sides of (i.e. above and below) the non-scanning voltage (either V5 or V2, depends on the polarity of scanning COM/row pulses). It is therefore desirable to provide a "floating" V_{BIAS} power supply system for the column/SEG switching needs (referring to Fig. 4a during each field in such a way that this "floating" power supply will substantially maintain its source voltage ($V_{B+}/V_{B0}/V_{B-}$, or V_{BIAS} for short) stability and supply the current necessary to support the electrode swing between V6-V4 during even fields and Vl-V3 during odd fields. With this "floating" V_{BIAS} power supply, then the IAPT folded driving scheme can be used and this allows a complete LCD driving system to be build using a single polarity LCD driving system to be built using twin-well CMOS process.

A preferred embodiment of this "floating" V_{BIAS} supply system 100 comprises a dedicated fixed high voltage V_{COM} power supply, a V_{BIAS} power supply and a switching circuit for generating certain appropriate electrical potentials for driving the COM or row and SEG or column electrodes. System 100 is shown in Fig. 4a, where node V6 is connected to a dedicated fixed high voltage V_{COM} power supply supplying a voltage V6, and nodes V3/V2/V1 are connected to a V_{BIAS} power supply to supply the three voltages V3/V2/V1. The voltage level for V1 is typically GND and V3-V2 = V2-V1 = V_{BIAS}. Control signal F2b is the inverse of F1b (Fig. 4b), with a tiny gap between the ON portions of these two signals to guarantee that no simultaneous turn ON of both power paths is possible.

In the odd fields, F2b is "1", switches I22, I24, I26 are ON, and capacitors C_{B+}/C_{B-} are connected to V3/V2/Vl, and system 100 will supply the voltage source to produce SEG/column driving signals between V1⇔V3, and COM/row scanning pulses between V2⇔V6.

In the even fields, Flb is "1", capacitors C_{B+}/C_{B-} are disconnected from V3/V2/Vl, and switch I23 connects the top terminal $C_{B+}t$ of C_{B+} to V6, which pulls up the other two terminals V_{bo}, C_B.b of capacitors C_{B+}/C_{B-}, assuming C_{B+}/C_{B-} capacitance is substantially higher than the loading current on nodes V5 and V4 generated by switching activities of SEG/column drivers I31/I32, then C_{B+}/C_{B-} will function as a steady voltage source for V5 and

V4 through switch I21 and I25. With V6, V5, V4, the system 100 driving SEG/column electrodes (only one pair of drivers is shown for one channel) will produce driving signals between V6⇔V4, while the system 100 will produce V5⇔Vl scanning pulses.

During the even field, since the SEG/column driving power comes entirely from capacitors C_{B+}/C_{B-}, for the above system to operate properly under all display patterns, the capacitance of C_{B+}/C_{B-} needs to be substantially (20x~50x) larger than (the sum of the pixel capacitance) x (maximum possible SEG/column electrode transitions). For a 100x200 pixel LCD panel assuming each pixel has a cell capacitance of 2pF, then the above calculation will imply the capacitance of C_{B+}/C_{B-} needs to be

(20x ~ 50x) x 2pF x 100x200x50 = 40 ~ 100uF,

where 50=100/2 is the maximum possible SEG/column transition,

happen when the pattern is black/white interleaved lines or checker board.

This capacitance requirement is very high and capacitors with such high capacitance values are generally high leakage, electrolytic type capacitors, and therefore are undesirable for ultra-low power battery operated devices.

An improvement based on the same circuit as the embodiment of Fig. 4a is to modify the power source management signal Flb/F2b, and insert "recharge pulses" in F2 pulses during the even field such that C_{B+}/C_{B-} will be recharged periodically (Fig. 4c). For example, by inserting such recharge pulses per row scanning period, the calculation for the capacitor required will reduce to: (20x ~ 50x) x 2pF x 100x200x50 / 100 = 0.4 ~ luF. This range of capacitance can be provided by ceramic capacitor which has negligible leakage current and are in very compact SMD (surface mount device) packages.

Another important factor for this scheme to function is the utilization of the intrinsic capacitances of LCD panels. During the brief periods where the recharging pulses are asserted during the even field, the intrinsic capacitance of the LCD performs as the holding capacitor for the SEG/column signal until capacitor C_{B+}/C_{B-} is reconnected to produce V5/V4. To achieve this, the output of SEG/column driver portion is temporarily turned off by setting both SS+ and SS- to "0", and therefore render the SEG/column drivers at a high impedance state to preserve the charge stored in the intrinsic capacitance of the LCD.

With the above structure, all control signals and switches will operate in the positive (or negative) voltage range (relative to GND). This is particularly advantageous where the structure is implemented as an integrated circuit, since the operating voltages can be all positive or negative in reference to the substrate potential. Therefore, other than the

capacitors C_{B+}/C_{B-}, all control signals and switches can be implemented by a conventional twin-Well CMOS process.

Practically all varieties of commercial passive LCD driving systems involve an orthogonal driving waveform which generally comprise a low voltage swing SEG/column driving system, and a high voltage pulses COM/row scanning system. The relative magnitude between SEG/column and COM/row scanning is generally decided by $\sqrt{Mux}$, where Mux is the multiplexing rate. For single row scanning system such as APT or IAPT driving schemes, the Mux rate equals the number of rows of the LCD. In MLA (multiple line addressing) driving schemes, Mux = Row/L, where L is the number of rows driven simultaneously at each row scanning period.

Because of significant difference of voltage levels between these two voltage requirements, it is usually undesirable to share one voltage supply between the SEG/column drivers and COM/row drivers. This invention introduces several embodiments for driving passive LCDs using two sets of power supplies to reduce the total power consumption of the LCD display system (including the power consumed by the LCD panel and by the driver). In addition, this invention describes several suitable circuit structures and control signal techniques for CMOS implementation to allow effective IC implementation of the introduced concept/method.

Although the above discussion is limited in its scope, the application of the power system structure system can be expanded to other types of passive LCD driving systems such as pulse-width modulation of SEG/column signals, frame-rate corrected gray-shade modulation and various MLA or active addressing methods. In each of the derived applications, the voltage levels need to be adjusted to optimally conserve the power, and the interaction with driving signals (especially SEG/column) needs to be properly managed to minimize the impact of the image quality.

In the embodiments of Figs. 3a-3d, a first power supply is used to supply electrical potentials dedicated for driving row or COM electrodes, and a second power supply separate from the first is used to generate electrical potentials dedicated and suitable for driving a column or SEG electrodes. In the embodiment of Figs. 4a-4c, however, it will be noted that the power sources V6, V3, V2 and V1 are used in combination for generating electrical potentials suitable for driving both row and column electrodes. Thus as described above, capacitors C_{B+}/C_{B-} in combination with the voltage sources V6, V3, V2 and V1 are used to

generate electrical potential V5 for driving the row electrodes as well as electrical potential V4 for driving the column electrodes.

It will be noted that in the description herein concerning embodiments employing capacitors, a power supply supplying a particular voltage is described as charging the capacitor to the same voltage. In practical circuits, however, it is understood that a capacitor is charged in a practical time frame to a desired voltage which is typically lower than the voltage supplied by the power supply. For example, if the two capacitors C_{B+} and C_{B-} are to be charged to 1.2 volts across each of the two capacitors, the voltage supply that is used to charge the two capacitors may need to supply a voltage of about 3.0 volts, rather than 2.4 volts in a practical implementation. It will be understood that, in all of the embodiments of the invention described herein involving the charging of capacitors, even though the description of such embodiments may indicate that the capacitors are charged to the same voltage as that supplied by the power supply, it will be understood that in actual practice, the two voltages are only substantially the same, preferably, with the voltage supplied by the power supply slightly higher than that of the desired voltage to which the capacitor is to be charged.

Figs. 5a and 5b together are a schematic circuit diagram of a power supply circuit for driving the LCD to illustrate the preferred embodiment of the invention. As shown in Figs. 5a and 5b, the overall circuit of the power supply system may be naturally divided into two portions: a first portion 200a for generating electrical potentials suitable for driving row and/or column electrodes and a second portion 200b for applying the electrical potentials supplied or generated by portion 200a to the row and column electrodes at the appropriate times. The first portion 200a is shown in Fig. 5a. As shown in Fig. 5a, three voltages are provided by two or more power sources: V6, VC and V1, where V1 may simply be ground potential. Two capacitors C1 and C2 are employed for storing energy during a first phase of the operation of combined circuit 200a, 200b. During the second phase, the energy stored in the capacitors is then used, together with the power sources V6, V1, for generating electrical potentials suitable for driving row and/or column electrodes.

The voltage VC is chosen so that the voltage difference between VC and V1 is substantially equal to the amplitude of the voltage difference between non-scanning row electrodes and column electrodes. Thus, during the first phase of operation of the combined circuit 200a, 200b, the control signal F3c is applied to switches I34, I36, I38 and I40, turning on these switches, so that capacitors C1 and C2 are connected in parallel to the voltage VC

and V1. Terminals C1t and C2t of C1 and C2 are thus charged to voltage VC and the remaining terminals C1b and C2b of the two capacitors are at the reference voltage V1.

During the second phase of the operation of the combined circuit 200a, 200b, control signal F3c is pulled low thereby turning off switches I34-I40. Then the control signal F1c or F2c is pulled high. Switches I44, I48 are of the type that they will turn on whenever either F1c or F2c is high. For convenience in description, it is assumed that F1c is pulled high first and not F2c. Then switches I42, I44, I48, I50, I56, I60, I64 and I68 are turned on. This causes terminal C1t of capacitor of C1 to be pulled to voltage V6. Since capacitor C1 has previously been charged during phase 1 to a voltage difference of (VC-V1) between its terminals, then the other terminal C1b of capacitor C1 is thereby also pulled to a value V5 so that the voltage difference (V6-V5) equals (VC-V1). The voltage V5, however, will be floating since it is not connected to any one of the three voltage supply nodes V6, VC and V1. Node VM will therefore be at voltage V5 through open switch I44. Terminal C2t of capacitor C2 is also connected to node VM so that it is pulled to voltage V5 and its other terminal C2b is pulled to a value V4 so that the voltage difference (V5-V4) is equal to the voltage difference (VC-V1). This is the case since the capacitor C2 has been charged during the previous phase 1 to this voltage difference. Thus, the voltage V5 passes through switch I44 and appears at node VM and the voltage V4 passes through switch I48 and appears at node 202.

In reference to Fig. 5b, the voltage V5 appearing in node VM passes through switch I56 and appears at node VC+ and reference voltage V1 passes through switch I60 to appear at node VC-. Therefore, by controlling switches I0 and I2 by means of control signals S+ and S- as before, the voltages V5 and V1 are applied to one or more COM or row electrodes. The voltage V6 also passes through switch I64 and appears at node VS+ and the voltage V4 at node 202 passes switch I68 to appear at node VS-. As before, by applying suitable timing control signals SS+(j) and SS-(j) to control switches I32 and I31, appropriate pulses of V6<=>V4 are applied to the corresponding column electrode SEGj. In reference to Fig. 2a, the above described driving voltage waveforms are the ones suitable for field 2xN, where the electrical potentials applied to the COM electrodes are between V5 and V1 and those applied to the column electrodes are between V6 and V4. As noted above, the voltages V5 and V4 are not connected to any power supply during this time and, therefore, float in reference to voltage V6 through the capacitors C1 and C2.

During the second phase, during another field addressing cycle, such as field 2xN+1 in Fig. 2a, the control signal F3c remains low, control signal F1c is pulled low and control

signal F2c is pulled high. This turns off switches I42, I48, I56, I60, I64 and I68, and turns on switches I46, I52, I54, I58, I62 and I66. Switches I44 and I50 remain on whenever either one of the control signals F1c and F2c is high. Terminal C2b of capacitor C2 is pulled to V1 through switch I52. Since the capacitor C2 has previously been charged during the first phase to (VC-V1), the terminal C2t will be pulled to a voltage V2 where (V2-V1) is equal to (VC-V1), where V2 floats in relation to V1 through capacitor C2. This voltage V2 passes switch I50 and appears at node VM. Terminal C1b of capacitor C1 is connected to VM through open switch I44 so that terminal C1b is also at voltage V2. Since the capacitor C1 has previously been charged to a value (VC-V1) during the first phase, the terminal C1t of capacitor C1 will be pulled to a value V3, where (V3-V2) is equal to (VC-V1), where V3, therefore, also floats with V2 and V1 through capacitors C1 and C2.

The voltage V3 passes through switch I46 and appears at node 204. In reference to Fig. 5b, voltage V2 appearing at node VM passes through switch I58 and appears at node VC- through switch I58 and the voltage V6 passes through switch I54 to appear at node VC+. Therefore, by means of timing control signals S+ and S-, the voltages V6 and V2 are applied through switches I0 and I2 to a selected COM electrode. Reference voltage V1 passes through switch I66 and appears at node VS- and the voltage V3 passes switch I62 to appear at node VS+. As before, by means of timing control signals SS+(j) and SS-(j) controlling switches I32 and I31, respectively, the voltages V3 and V1 are applied to the corresponding electrode SEGj, where j ranges from 1 to the maximum number of column electrodes, such as k in Fig. 1. The operation of the combined circuit 200a, 200b of Figs. 5a, 5b during the two phases is summarized in the table below, where the underlined voltages are the ones that are floating:

	F3c	F1c	F2c
C1t	VC	V6	<u>V3</u>
C1b	V1	<u>V5</u> (V_c-V_1=V_6-V_5)	<u>V2</u> (V_c-V_1=V_3-V_2)
C2t	VC	<u>V5</u>	<u>V2</u> (V_c-V_1=V_2-V_1)
C2b	V1	<u>V4</u> (V_c-V_1=V_5-V_4)	V1

With the above structure in Figs. 5a, 5b, all control signals and switches will operate in the positive (or negative) voltage range (relative to GND). This is particularly advantageous where the structure is implemented as a single-chip integrated CMOS circuit, since the operating voltages can be all positive or negative in reference to the substrate

potential. Therefore, other than the capacitors C1 and C2, all control signals and switches can be implemented by a conventional twin-Well CMOS process.

In the embodiment of Figs. 5a, 5b, the operation of the circuit has two distinct phases: a first phase during which one or more capacitors is charged and during which no electrical potentials are applied to the row or column electrodes. This is followed by phase 2 where one of the two terminals of each capacitor is connected to a voltage supply so that the electrical potential of the remaining terminal of the capacitor is pulled to a value equal to the voltage difference (VC-V1) from that of the voltage supply. One or more of the voltage supplies V6 and V1 from the power supplies and one or more of the generated floating voltages at such other terminal of each of the two capacitors are then used to control and drive the row and column electrodes.

In other embodiments described above, such as those in Figs. 3c, 3d and 4a, there are also two phases where during the first phase, one or more capacitors is charged, and where during the second phase, a floating voltage at a terminal of the capacitor(s) and one or more supply voltages are used for driving row and/or column electrodes. In such embodiments, however, the supply voltage or voltages are also used during the first phase to drive the row and/or the column electrodes. All such variations are within the scope of the invention.

In the embodiment of Fig. 4a, it may be important to employ capacitors C_{B+} and C_{B-} that are of substantially equal value and employ voltage supplies V3, V2, V1 so that (V3-V2) is substantially the same as (V2-V1). This is the case to maintain a zero voltage offset at the column electrodes. In the embodiment of Figs. 5a, 5b, this is assured since the capacitors C1 and C2 are charged in parallel during the first phase to the same voltage difference. This reduces the tolerances for components that may be used in the drivers so that lower cost components may be used. In the embodiment of Fig. 4a, the two capacitors are charged when they are placed in series whereas in the embodiment of Figs. 5a, 5b, the two capacitors C1 and C2 are charged when there placed in parallel between the same two voltage sources.

Thus, the feature common to the embodiments in Figs. 3c, 3d, 4a, 5a and 5b is that two or more power supplies together with a circuit including an energy storage device are employed to generate electrical potentials for driving row and column electrodes. The circuit causes at least one of the electrical potentials so generated to float with a voltage supplied by one of the power supplies. Thus, in the embodiment of Figs. 3c, 3d, when the reference voltage V0 is connected to node V+, thereby putting one terminal of the capacitor C0 to the reference voltage, the other terminal of capacitor C0 is pulled to the floating value - V_{COM+} or V_{COM-}.

In the embodiment of Fig. 4a, when the capacitors C_{B+} and C_{B-} are pulled up by voltage supply V6, this causes the node between the two capacitors and the remaining terminal of capacitor C_{B-} to also be pulled to floating values useful for driving the row or column electrodes. Thus, the voltage value at the node between the two capacitors is pulled to a value V5 where (V6-V5) is substantially equal to (V3-V2) which is the voltage difference by which the capacitor C_{B+} has been charged during the previous phase. At the same time, the voltage at node VS- will also be pulled up to the voltage at the bottom terminal C_{B-t} which is at a voltage V4, where (V5-V4) is substantially the same as (V2-V1). This is the case since capacitor C_{B-} has previously been charged during the previous phase to (V2-V1).

Yet another feature common to the embodiments of the invention in Figs. 3c, 3d, 4a, 5a and 5b is that the driver circuit as a whole experiences a voltage dynamic range which does not substantially exceed the amplitude of the voltage pulses applied to the row electrodes. In reference to Fig. 2b, for example, where two separate voltage sources are employed to generated the positive and negative going voltage pulses for application to row electrodes, the power supply circuit would experience a voltage dynamic range equal to the sum of the amplitudes of the positive and negative going pulses. Since the positive and negative going pulses should have equal amplitudes for zero DC offset, this means that such power circuit would experience twice the amplitude of the voltage pulses applied to the row electrodes. In the example shown in Fig. 2b, the dynamic range experienced by the power circuit would be equal to V_{COM+}, which is equal to V_{COM-}. In the embodiments of Figs. 3c, 3d, 4a, 5a and 5b, since capacitors have been used to enable a single power supply to generate both the positive and negative going voltage pulses for row electrodes, the voltage dynamic range seen or experienced by the power supply circuit as a whole is substantially equal or not significantly higher than the amplitude of the positive and negative going pulses applied to the row electrodes. In other words, such feature enables the total voltage dynamic range to be reduced as in the case of IAPT, while at the same time vastly reducing the power consumption by the driver when compared to IAPT.

From the description above, it will be evident since the column (SEG) electrodes are driven either directly by a reference voltage (from a power source or supply, or connected to ground or other reference source) or directly by an energy storage device such as a capacitor (or inductor), so that the above-described problems associated with Class B bias circuits are avoided altogether. It is due to the fact that the driver circuits described above do not employ N and P transistors that are turned off at low error voltage for supplying energy to the column

electrodes. Thus, assuming that the energy storage sources are able to drive the column electrodes to substantially their target values within each row scanning cycle, the above described crosstalk problem exhibited by conventional LCDs is avoided or alleviated.

Where energy storage devices such as capacitors are used to supply current to column electrodes, in order to drive the column electrodes to target voltage values, the accuracy at which these target values can be accomplished depends on the capacitance of the driving capacitor relative to the load capacitance of the column electrode that is driven by means of the capacitor. Thus, if the capacitance of the driving capacitor is 20 times that of the load capacitance at the column electrode being driven, the capacitor can drive the column electrode to within 5 percent of the target voltage value. Thus, in order to further increase driving accuracy so that the error is less than 5%, even larger capacitors may need to be used. Another aspect of the invention is based on the recognition that, by using two or more sets of capacitors to drive the column electrode during the same row-scanning period, the above requirement of using large value capacitors for achieving accurate target values may be relaxed. According to this aspect of the invention, a column electrode may be driven by a first set of one or more capacitors to a voltage value which is close to but not at the target value, and then a second set of one or more capacitors is then used to drive the column electrode to substantially the target value. Using such driving scheme, the capacitances of the capacitors in the first and second sets need not be huge. For example, if the capacitances of capacitors in the first and second sets are each 20 times or more than the load capacitance, then during the first phase, the column electrode is driven to within 5 percent of the target value. During the second phase of the same row-scanning cycle, the second set of capacitors is then used to drive the column electrode to within 0.25 percent of the target value, or substantially at the target value.

This aspect of the invention is illustrated in Figs. 6a, 6b. As shown in Fig. 6a, circuit 300 includes a power supply 302 which includes a current source 304, a comparator 306 and a reference voltage 308. Voltage reference source 308 provides a reference voltage V_{REF} relative to the ground. Circuit 300 includes two sets of capacitors: a first set comprising capacitors C1, C2 and a second set comprising capacitors C3, C4. The two sets of capacitors are used alternately to supply voltages or electrical potentials to three nodes: N1, N2 and N3. The voltages or electrical potentials at these three nodes are then used for driving each of the column electrodes (SEG) to one of a set of three different potentials as required: V1, V2 and V3. The same scheme may be used for achieving the set of potentials V4, V5 and V6 as well.

When the first set of capacitors is being used to supply current to the three nodes, the second set of capacitors is connected to the power source or supply 302 for charging the second set of capacitors. This occurs during one cycle of the switching circuit 300. During the next cycle, the second set of capacitors is then used to supply power to the three nodes while the first set of capacitors is then charged by the power supply 302. The operation of the switches and the alternate operation of the two sets of capacitors are illustrated in reference to the timing diagram of Fig. 6b.

Circuit 300 may be operated in two different operations illustrating two different embodiments. The first embodiment is illustrated by the timing diagram 320 labeled S1 through S4, which are graphical illustrations of the On-Off states of the switches S1-S4 of circuit 300. The second set of timing diagrams 330 and labeled S1', S2, S3' and S4 illustrate a second embodiment in operating circuit 300.

Each of the two dotted lines t0 and t0' marks the starting point in time of the scanning of a new line or row electrode. Thus the time period t0-t0' defines a row-scanning period or a row-scanning cycle. During a row-scanning cycle, it is desirable for power supplied by circuit 300 to drive each of the column electrodes to the target voltage or electrical potential as quickly as possible. During the row-scanning cycle t0-t0', the switches S1 and S4 are turned off during a greater part of the cycle and switches S2 and S3 are turned on. Thus, during a greater part of the cycle, the second set of capacitors C3, C4 are connected to nodes N1, N2, N3 and disconnected from the power supply 302. For example, node C3t is connected to node N1 and node C3b is connected to node N2. Node C4t is connected to node N2 and node C4b is connected to node N3. Therefore, the potential difference or voltage across nodes N1, N2 is substantially equal to the voltage across capacitor C1, and the voltage across nodes N2, N3 is substantially equal to the voltage across capacitor C2. Since switches S4 are off most of the time during this row-scanning cycle t0-t0', capacitors C3, C4 are not connected to the power supply 302 during a greater portion of this row-scanning cycle.

In the same vein, since switches S4 are turned off and switches S3 are turned on during a greater part of the cycle, the first set of switches is disconnected from the nodes N1-N3 and connected to the power supply in order to replenish the charges in the capacitors that were drained during the previous row-scanning cycle. In this manner, during the row-scanning cycle immediately following time t0', the first set of capacitors would be fully charged and then ready to supply energy to nodes N1, N2, N3.

While it is true that during a major portion of the row-scanning cycle t0, t0' the second set of switches are connected to nodes N1-N3 and the first set of switches are connected to

the power supply 302, it will be observed from Fig. 6b that the switching cycle S1-S4 are delayed by an offset t0-t1 relative to the starting time t0 of the row-scanning cycle. This is preferable to achieve a greater accuracy for driving column electrodes connected to nodes N1, N2, N3 to the desired target voltage values. As shown in Fig. 6b, in order to drive a column electrode from voltage V1 to voltage V3, for example, the first set of capacitors C1, C2 is still connected to nodes N1, N2, N3 at time t0. In fact, as will be explained below, during this short time period t0-t1 that makes up only a small portion of the row-scanning cycle t0-t0', a major portion of the charges originally stored in capacitors C1, C2 is now transferred during this short time period to the column electrode by circuit 300 as shown in curve Emb.1 in Fig. 6b. Thus, at time t1, the voltage of the column electrode connected to circuit 300 is driven from a value of V1 at time t0 to a value V' which is close to the target voltage V3 at time t1. At time t1, switches S1, S4 are turned off and switches S2, S3 are turned on. This causes capacitors C1, C2 to be disconnected from nodes N1-N3 and capacitors C3, C4 to be connected to the nodes instead. At this time t1, capacitors C3, C4 have been fully charged by the power supply 302 and are therefore very effective in quickly driving the same column electrode that was driven to voltage V' by C1 and C2 to a value very close to the target voltage V3, as shown in curve Emb.1 in Fig. 6b.

For example, if the capacitance of capacitors C1, C2 is 20 times that of the load capacitance, this means that V' will be less than V3 by only about 5 percent or so of V3. If the capacitance of capacitors C3, C4 is also 20 times that of the load capacitance, this means that when the second set of capacitors is used to drive the same column electrode from V' towards voltage V3, the resulting voltage of the column electrode will be within about 0.25 percent less than V3. In this manner, the column electrode can be driven to a voltage substantially equal to the target voltage value without having to use large value capacitors.

From the above, since the column electrode is already driven to the voltage V' by capacitors C1, C2, where V' is close to the voltage V3, the second set of capacitors C3, C4 will only need to supply a small amount of charge and current in order to drive such column electrode towards the value substantially equal to V3. Therefore, at time t0', only a minor portion of the charges have been drained from capacitors C3, C4. Therefore, during the subsequent short time period t0'-t1', a major portion of such charges will then be transferred to the column electrode connected to nodes N1-N3, in order to again drive such column electrode to a voltage value which is close to voltage V3, or some other target voltage.

In the example illustrated above, the column electrode is driven from voltage V1 to a voltage substantially equal to voltage V3. The same reasoning will apply for the two sets of

capacitors to drive any column electrode from any one of the three voltage values V1-V3 to another different voltage value with all the associated advantages explained above.

Thus, as will be evident from the above, by delaying the timing of the switching cycle 320 relative to the row-scanning cycle by an offset t0-t1, t0'-t1', ..., the column electrodes may be driven to values very close to or substantially equal to the target voltage without having to use large-size capacitors.

The second embodiment 330 differs from the first embodiment 320 in that the starting points of time periods in which the first set of capacitors C1, C2 is turned off is furthered delayed to times t2, t2', ... as illustrated by the timing S1'. Thus, during the time period t1-t2, both sets of capacitors C1-C4 will be supplying current and energy to the three nodes, thereby shortening the time which is required to drive a column electrode connected to the nodes to a value substantially equal to V3. The overlapping time period is shown as shaded areas in the waveform 330. The resulting voltage of the column electrode is illustrated by curve Emb. 2 in Fig. 6b.

As will be noted from the switching waveforms 320, 330, the three pairs of switching waveforms S1, S3; S2, S4 and S1', S3' are complementary. In this manner, when a set of capacitors is connected to the nodes to supply energy to the column electrodes, this set is disconnected from the power supply; vice versa, when a set of capacitors is connected to the power supply 302 in order to charge the capacitors, this set is disconnected from the nodes.

Power supply 302 operates as follows. Current source 304 will supply current to one of the two sets of capacitors connected to it until it is switched off by comparator 306. When switches S3 are on, comparator 306 compares the common voltage at node C1t, C2t for the first set of capacitors to the voltage reference V_{REF}. When the voltage at the common node is raised by the charging action so that it is substantially equal to the reference voltage, comparator 306 turns off the current source 304. During this charging process, capacitors C1, C2 are connected in parallel to the current source 304. Capacitors C3, C4 are charged in a similar manner.

After the charging process, the voltage across each of the capacitors C1-C4 is substantially equal to the reference voltage V_{REF}. Therefore, when the fully charged capacitors are then connected to nodes N1-N3, the voltage across nodes N1, N2 and across nodes N2, N3 would each be substantially equal to the reference voltage V_{REF}.

While two sets of capacitors are employed as illustrated in Fig. 6a, 6b, it will be understood that a single set may be adequate for some applications, and that more than two

sets may be used in other applications; such other variations are within the scope of the invention.

While the invention has been described above by reference to various embodiments, it will be understood that changes and modifications may be made without departing from the scope of the invention, which is to be defined only by the appended claims and their equivalents. All references referred to herein are incorporated by reference in their entireties.